CLAIMS:

1. A wafer bonding method, comprising:

forming an interlevel dielectric (ILD) on opposing surfaces of adjacent wafers each wafer including one or more active integrated circuit (IC) devices;

selectively depositing metallic lines, via the ILD, on opposing surfaces of the adjacent wafers;

selectively recessing the ILD surrounding the metallic lines deposited via the ILD to facilitate direct metal bonding between the adjacent wafers;

selectively aligning the adjacent wafers to form a stack; and

bonding the metallic lines on the surface of one wafer with the metallic lines on the surface of the other wafer to establish electrical connections between active IC devices on the adjacent wafers.

2. The wafer bonding method as claimed in claim 1, wherein the metallic lines are Copper (Cu) bonding pads deposited on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers.

3. The wafer bonding method as claimed in claim 1, wherein the ILD recess is

created by a Chemical Mechanical Polish (CMP).

4. The wafer bonding method as claimed in claim 1, wherein the ILD recess is created by selectively etching the ILD surrounding the metallic lines deposited via the ILD.

5. The wafer bonding method as claimed in claim 1, wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded.

6. The wafer bonding method as claimed in claim 5, wherein the high-temperature deformable dielectric is SILK which exhibits a glass transition near 450^0C while the metallic lines exhibit a bonding temperature of about 400^0C.

7. The wafer bonding method as claimed in claim 1, wherein the one wafer is thinner than the other wafer to conform to height differences of the metallic lines across opposing surfaces of the adjacent wafers.

8. A three-dimensional (3-D) integrated chip system, comprising:

a first wafer including one or more integrated circuit (IC) devices, metallic lines deposited via an interlevel dielectric (ILD) for wafer-to-wafer bonding and electrical interconnection, and

an ILD recess surrounding the metallic lines deposited via the ILD; and

a second wafer including one or more integrated circuit (IC) devices, metallic lines deposited via an interlevel dielectric (ILD) for wafer-to-wafer bonding and electrical interconnection, and an ILD recess surrounding the metallic lines deposited via the ILD, wherein the metallic lines on the surface of the second wafer are bonded with the metallic lines on the surface of the first wafer to establish electrical connections between active IC devices on the adjacent wafers.

9. The three-dimensional (3-D) integrated chip system as claimed in claim 8, wherein the metallic lines include Copper (Cu) bonding pads deposited on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers.

10. The three-dimensional (3-D) integrated chip system as claimed in claim 8, wherein the ILD recess is created by a Chemical Mechanical Polish (CMP).

11. The three-dimensional (3-D) integrated chip system as claimed in claim 8, wherein the ILD recess is created by selectively etching the ILD surrounding the metallic lines deposited via the ILD.

12. The three-dimensional (3-D) integrated chip system as claimed in claim 8, wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded.

13. The three-dimensional (3-D) integrated chip system as claimed in claim 12, wherein the high-temperature deformable dielectric is SILK which exhibits a glass transition near 450^0C while the metallic lines exhibit a bonding temperature of about 400^0C.

14. A three-dimensional (3-D) integrated chip system, comprising:

a first wafer including one or more integrated circuit (IC) devices;

a second wafer including one or more integrated circuit (IC) devices; and

metallic lines deposited on opposing surfaces of the first and second wafers at designated locations with an interlevel dielectric (ILD) recess surrounding the metallic lines to facilitate direct metal bonding between the first and second wafers and establish electrical connections between active IC devices on the first and second wafers.

15. The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the metallic lines include a plurality of Copper (Cu) bonding pads on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers.

16. The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the ILD recess is created by a Chemical Mechanical Polish (CMP).

17. The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the ILD recess is created by selectively etching the ILD surrounding the metallic lines deposited via the ILD.

18. The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded.

19. The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the high-temperature deformable dielectric is SILK which exhibits a glass transition near 450^0C while the metallic lines exhibit a bonding temperature of about 400^0C.

20. The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the first wafer is thinner than the second wafer to conform to height differences of the metallic lines across opposing surfaces of the adjacent wafers.